Controlling and Driving the SEPIC

— NON-PUBLISHED NOTES & REFERENCES —
— WORK-IN-PROGRESS —

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Abstract

Investigating the "Single Ended Primary Inductor Converter" for use with residential, rooftop, commercial or industrial solar panels. The purpose of this study is to gain a more thorough understanding of the theory of operation of switching power supplies and "charge controllers" for solar panel systems before putting it in practice.

Please do your own research. Fully hyperlinked references are included for convenience.

Contents

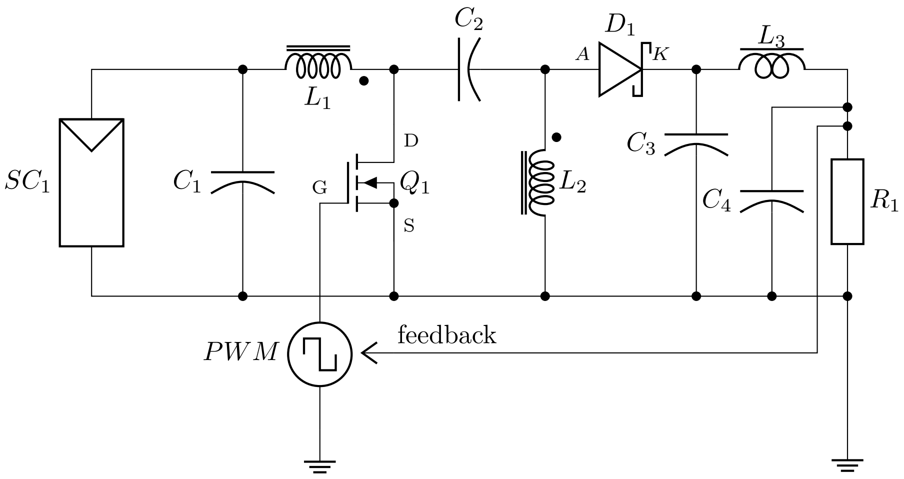

Figure 1: SEPIC circuit diagram

1 Introduction

The SEPIC [8] is one of a number of regulated switching power supply topologies, among which are included various versions of Buck, Boost, Buck–Boost, Flyback, Zeta and Ćuk[1] DC-to-DC converters, to name a few as if one would have attended a conference or presentation in Las Vegas on various get-rich-quick schemes.

We are confronting a pernicious problem with obnoxious patent issuances and intellectual property lawsuits over standard, commonly taught, well-known, and legally unpatentable designs. When obnoxious patents are licensed as intellectual property, and royalties are collected, the patented inventions tend to be manufactured under paid suit-and-tie licenses and shady contracts with substandard parts and sold as consumer junk.

We have not been seeing the quality we are after, particularly the details of filtering and smoothing the power supply, including the LC filter on the output in Figure 1, which is omitted in most introductory diagrams, but really essential in practice [9], probably with some field testing.

2 Discussion of the SEPIC topology

If the inductors L_1 and L_2 in Figure 1 are coupled, or wound on the same iron core as indicated by the black dots in the diagram, then the capacitors C_1 and C_2 are essentially placed in parallel, and one or the other may be removed

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[1] Named after the prolific Serbo-Croatian–American inventor Slobodan Ćuk of the California Institute of Technology.

without affecting the circuit much, because the inductance in canceled out for any electric current flowing through L_1 and back the opposite way through L_2. Nevertheless, the capacitors C_1 and C_2 as placed serve to protect the power MOSFET Q_1 from transient “spikes” in the inductive windings.

When Q_1 is switched on by the PWM, the current through L_1 increases, and when Q_1 is switched off, the remaining magnetic flux in the iron core forces the current through the other winding L_2 past the diode D_1 to keep the capacitor C_3 charged and continue supplying power to the load resistance R_1. This is omitting C_2 from consideration, and depending on mutual inductance alone.

However the circuit will still function if the inductors L_1 and L_2 are *not* coupled and C_2 is present. See [4]. In this case, C_2 is discharged by current flowing through L_2 when Q_1 is switched on, and additional supply current is admitted through L_1. Now when Q_1 is switched off, C_2 is charged again by current continuing through L_1, and the current that was flowing through L_2 as C_2 was discharging is suddenly switched and forced through the diode D_1 instead.

When the inductors L_1 and L_2 are coupled, and C_2 is present, there is additional redundancy, stability, and reliability for the circuit.

3 Calculating the duty cycle of the PWM

A simple way to figure out the duty cycle of the pulse width modulator needed to produce the desired potential at the output is to consider that the mean potential at the drain of Q_1 over the switching cycle must be equal to the input potential V_1, and that potential is equal to zero, or the forward voltage drop of the transistor during the time when it is on, which we want as small as possible. That potential must then be high enough during the time when the transistor is off to average out to the correct value over the entire clock cycle T. Let τ be the pulse width, or the time when the power transistor Q_1 is turned on and conducting electricity between its source and drain:

$$\overline{V_Q} = V_1; \qquad V_{Q\text{on}} = 0; \qquad V_{Q\text{off}} = \frac{TV_1}{T-\tau}.$$

Now consider the operating potential V_P at the anode A of diode D_1. At all times, V_P is less than the potential V_Q at the transistor drain by a difference equal to the input potential V_1.

$$V_P = V_Q - V_1.$$

So

$$\overline{V_P} = 0; \qquad V_{P\text{on}} = -V_1; \qquad V_{P\text{off}} = \frac{\tau V_1}{T-\tau}.$$

Increasing the duty cycle τ/T will increase the potential $V_{P\text{off}}$ which is available at the output less the forward drop through the diode D_1, but it will correspondingly decrease the clock-cycle-averaged current available at the increased potential. A Pulse Width Modulator with a feedback loop will assist in maintaining a stable output potential from a variable input potential from solar panels.

4 Energy transfer per clock cycle

The amount of energy stored in an capacitor or inductor, respectively, is:

$$E_C = \frac{1}{2}V^2C; \qquad E_L = \frac{1}{2}I^2L.$$

Zhang [24] suggests choosing inductors of a value that will allow a 40% ripple in current at the switching frequency. In effect, that causes perhaps 64% of the total energy stored in an inductor to be transferred each clock cycle, which appears to be a good practical limit of tolerable "ripple" under conditions of light load or open circuit among other considerations.

We suggest using heavy gauge wire on a heavy iron core to carry large currents to avoid overheating and/or saturating the core. This only permits relatively few turns of wire and will not result in any excessively large inductance.

The capacitors in a coupled SEPIC system are movable, and their exact values do not seem to be critical.

5 Size and scale of systems proposed

We propose off-grid solar electric power systems for use by "sovereign citizens" or "freemen on the land" (or even banks or broker houses that desire back-up power and money savings at the city electric meter) with about a dozen solar panels rated at 18 V and 200 W each, all connected in parallel to serve a common automotive-like 12 V electrical system for which many accessories are commonly available, as well as inverters to produce 110 VAC if desired.

6 Selection of components and bill of materials

The selection of components is based on how much "'ripple voltage" and possible overheating of components we are willing to tolerate versus how much money we can afford and are willing to spend on bigger and better components for reliability and smoothness of the power supply system.

6.1 Power MOSFETs or IGBTs

For Q_1 in Figure 1, the Littelfuse/IXYS IXFN520N075T2 [6] or the Vishay VS-FC420SA10 [23] might be useful. IGBTs are better than MOSFETs for higher frequency switching but are much less desireable for a low-voltage system because of a greater forward voltage drop. On the other hand, the higher gate voltage required to turn them on is a possible disadvantage of MOSFETs.

6.2 Power Schottky rectifier diodes

The ST Microelectronics STPS200170TV1 [11] and the Vishay VS-203CNQ100PbF [22] are likely candidates.

6.3 Power audio capacitors

We suggest using power audio capacitors from a music supply store [1, 2] for the capacitors C_1, C_2 and C_3 in Figure 1, and certainly for that matter our proposed system will be capable of powering the high-end stereo systems offered at those stores. Check ratings carefully for use with 18–24 V. It may be possible to use two identical capacitors in series to double the voltage rating. Some care will be needed to switch them on to avoid a short-circuit inrush current.

6.4 Heavy iron inductors and power chokes

Inductors and chokes are to be wound by hand with varnished magnet wire of adquate gauge on suitably heavy toroidal cores of laminated mild electrical steel or ferrite to prevent saturation in normal use. The use of closed toroidal cores reduces radio and audio systems interference.

6.5 Pulse Width Modulators

We suggest a Texas Instruments line-up of pulse width modulators depending on the desired frequency.

6.5.1 High frequency

The LM515xx series [12, 13, 16, 14, 15] of pulse width modulators offer a dynamically programmable switching frequency ranging from 100 kHz to 2.2 MHz. Switching in the megahertz range for our application may incur excessive power losses and inefficiency in the large power MOSFETs [11, 22], although the reason high frequencies have been used for this purpose was to enable a greater power transfer through inductors and capacitors that can hold only a fixed amount of energy per clock cycle.

6.5.2 Medium frequency

The TL5001xx series PWMs [18, 19, 21, 20] operate in the range of 20 kHz to 500 kHz. These chips are older, rather outdated, and no longer under active development, but they are still in production.

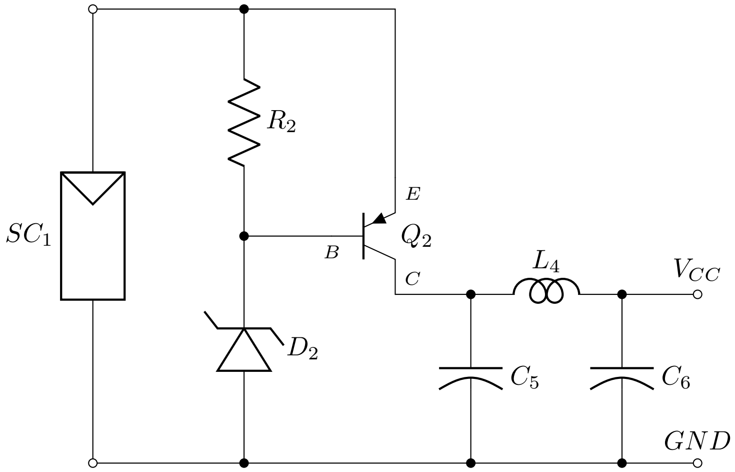

Figure 2: Logic level power supply for PWM

6.5.3 Low frequency

The LM555 [17] or similar ICs from many manufacturers may be used for frequencies below 20 kHz, but the 555 is a general purpose timer which will require additional customization and circuitry to use specifically for pulse width modulation. There is no reason we cannot go as low as 400, 60 or even 50 Hz. Larger inductors and capacitors will be required in these cases, but the converter will be more efficient and may produce smoother, cleaner power.

The “Arduino” also has a rudimentary pulse width modulation “analog output” running at about 0.5 kHz [5], which is adequate for our purposes as long as we design and plan for the very low frequency.

6.6 Logic level power supply

A simple Zener diode voltage regulator with a transistor current buffer [7] as depicted in Figure 2 should be used to power logic level circuits directly from highly variable power supplies if possible. This simple circuit also has the effect of an undervoltage lockout or UVLO [3]. Some hysteresis [10] would be desirable in order to avoid an amplified chattering effect from transistor Q_2 when the voltage supply is barely adequate and teetering at the edge of the lockout level.

6.7 The feedback loop

There needs to be a stable and reliable automated method of adjusting the duty cycle of the PWM up and down between certain limits based on the difference between the desired correct output voltage and the actual output voltage measured.

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